REMARKS

Summary

Claims 4, 9, 12, 16 and 18 are currently amended. No new matter was added as a result.

Drawing Objections

The Examiner objected to Figures 5, 6, 8, and 9 arguing that they are captures of a digital oscilloscope making it difficult to differentiate between the signals. However, digital oscilloscopes are commonly used, and one of ordinary skill in the art would be able to look at the oscilloscope captures and differentiate between the signals. Also, references pointing out the specific signals aid in the differentiation of the signals. Figures 5 and 8 were objected to for not providing any references. Replacement Sheets are attached to address the objection.

Claim Objections

Claims 4 – 6 were objected to because of the following informalities: "the reset circuit in claim 4 actually includes the elements of the filtering circuit, as clearly described in the specification (paragraphs 37 – 38)." (Office Action, page 3).

Claim 4 is currently amended, as shown above, addressing the informalities cited by the Examiner. Therefore, currently amended claim 4 is allowable.

Claims 5 and 6 depend from currently amended and allowable claim 4 and, therefore, are allowable for at least this reason.

Pursuant to 37 C.F.R. § 1.111, Applicant respectfully requests reconsideration of the claim rejections set forth in the Office Action dated October 18, 2006.

Claim Rejections

Claims 7, 8 and 15 – 19 were rejected under 35 U.S.C § 103(a) as being unpatentable over Koga et al. (U.S. Patent 6,894,673) in view of Admitted Prior Art.

In regards to claim 7, the Examiner argues that Koga et al. teaches all the claim limitations except the "timing controller including an electrostatic protection circuit" and that the "GOE mask time of the GOE signal to be longer than about 16 msec." (Office Action, pages 4 – 5).

However, Koga et al. also does not teach that the "filtering circuit ... reducing an impulse of the clock signal." Nevertheless, the Examiner argues that reducing an impulse of the clock signal is shown by Koga et al. (Figure 7 and column 9, lines 1 – 33). (Office Action, page 5). Yet, nothing in the Figures or the specification describes or shows an impulse of a clock signal that is physically reduced due to a filtering circuit. The Examiner merely argues that a gate driver output enable signal ("VOE") causes a vertical clock signal ("VCK") and corresponding data latch pulse signal ("DLP") to shift or delay. (Office Action, page 5). Firstly, the VOE is causing the shift or delay, not the filtering circuit, unlike the Applicant's claimed device where the filtering circuit reduces an impulse of the clock signal. Secondly, a shift or delay of a signal is not the same as having an impulse on a signal and reducing that impulse. Therefore, Koga et al. does not teach the limitation that a "filtering circuit ... reducing an impulse of the clock signal."

In regards to the claimed limitation that the "GOE mask time of the GOE signal to be longer than about 16 msec," the Examiner admits that Koga et al. does not teach this. (Office Action, page 5). Also the Admitted Prior Art does not teach this. Yet the Examiner argues that it is understood that the minimum time is to be set according to factors such as frame rate, color depth, display resolution, etc. and concluding that it would have been obvious to one of ordinary skill in the art to set a minimum mask duration to provide optimal display. (Office Action, page 5).

Firstly, "to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." MPEP § 2143.03. The Examiner does not show that the prior art teaches or suggests a minimum time to be set.

Secondly, the Applicant is claiming a specific minimum time that addresses a particular problem. The claimed limitation specifically recites a GOE mask time of the GOE signal to be longer than about 16 msec. The 16 msec is a definite and unique time boundary. For example, the Applicant's specification, paragraph 13, shows that a short duration of the GOE signal may cause an abnormal operation of the gate driver, thereby the LCD panel may abnormally display images. Then in paragraph 40 of the Applicant's specification, the Applicant describes that a GOE mask time duration longer than about 16 msec allows images to be normally displayed.

Koga et al. in combination with the Admitted Prior Art does not teach all the elements of claim 7. Accordingly, the prima facie case for obviousness has not been met. Therefore, claim 7 is allowable over the cited references.

Claim 8 depends from allowable claim 7 and, therefore, is allowable for at least this reason.

Claim 8 is allowable for additional reasons that are independent of the reasons set forth above. Claim 8 recites, *inter alia*, that a digital input voltage (DVCC) is applied to the electrostatic protection circuit and the filtering circuit. The Examiner argues that even though the Admitted Prior Art and Koga et al. do not teach DVCC being applied to the filtering circuit, one of ordinary skill in the art would recognize the basic need of a power supply voltage to a circuit to provide power and/or a reference level for operation. (Office Action, page 6). However, the claimed limitation is not just reciting that a power supply should be applied to a filtering circuit, but, instead, it is specifically reciting that the same DVCC is to be applied to both the electrostatic protection circuit and the filtering circuit.

Claims 9 and 10 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 is currently amended to incorporate the limitations of claims 10 and 11, as shown above. The Examiner admits that claim 11 would be allowable if rewritten. (Office Action, page 9). Therefore, currently amended claim 9 is allowable.

Claims 10 and 11 are canceled.

Claims 12 – 14 are dependent on currently amended claim 9 and, therefore, are allowable for at least this reason.

Claim 15 depends from allowable claim 8 and, therefore, is allowable for at least this reason.

Claims 16 – 19 were rejected similarly per the rejection analyses of claim 7. However, claims 16 and 18 are currently amended, as shown above, and, therefore, are allowable for based on the same arguments made in regards to claim 7.

Claims 17 and 19 are canceled, rendering the respective rejections moot.

Claims 7, 8 and 15 – 19 were also rejected under 35 U.S.C § 103(a) as being unpatentable over Shin (JP 11-249613) in view of Admitted Prior Art.

In regards to claim 7, the Examiner argues that Shin teaches all the claim limitations except the "timing controller including an electrostatic protection circuit" and that the "GOE mask time of the GOE signal to be longer than about 16 msec." (Office Action, page 7).

However, the Examiner argues that Shin teaches a LCD module including a gate driver and a source driver, where the gate and source driver are inherent. (Office Action, page 7). Just because a reference teaches a LCD module, it is not inherent that

the LCD module includes a gate driver or a source driver or any driver for that matter. It is possible that other techniques and devices may be used to operate a LCD module other than drivers. Neither the Figures nor specification of Shin disclose a driver. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999); MPEP § 2112, part IV.

Also, Shin does not teach that the "filtering circuit ... reducing an impulse of the clock signal." Nevertheless, the Examiner argues that reducing an impulse of the clock signal is shown by Shin (Figures 2 and 3, paragraphs 34-41). (Office Action, page 7). Yet, nothing in the Figures or the specification describes or shows an impulse of a clock signal that is physically reduced due to a filtering circuit. The Examiner argues that when a Mask signal is low, an ENB1 signal is masked resulting in an inactive ENB2 signal. (Office Action, page 7). Yet, the figures show that the ENB1 signal is not reduced, but, instead, the Mask signal is used to activate the ENB2 signal during specific portions of the ENB1 signal. Using specific timing signals to activate a gate driver signal, ENB2, at desired times is not the same as having an impulse on a signal and reducing that impulse. Therefore, Shin does not teach the limitation that a "filtering circuit ... reducing an impulse of the clock signal."

In regards to the claimed limitation that the "GOE mask time of the GOE signal to be longer than about 16 msec," the Examiner admits that Shin does not teach this. (Office Action, page 7 – 8). Also the Admitted Prior Art does not teach this. Yet the Examiner argues, pointing to nothing, that it is understood that the minimum time is to be set according to various display requirements and concluding that it would have been obvious to one of ordinary skill in the art to set a minimum mask duration in order to provide optimal display. (Office Action, page 8).

The same arguments regarding the claimed limitation that the GOE mask time of the GOE signal to be longer than about 16 msec, as discussed above concerning Koga et al., apply here. Accordingly, the prima facie case for obviousness has not been met. Therefore, claim 7 is allowable over the cited references.

The Examiner uses the same rejection analysis for claims 8, 15, and 16 – 19, using Shin as was done above in regards to Koga et al. Therefore, the arguments made above in regards to Koga et al. apply here. Accordingly, claims 8, 15, 16 and 18 are allowable.

Conclusion

For at least the reasons presented above, the Applicant respectfully submits that the pending claims are in condition for allowance.

The Examiner is respectfully requested to contact the undersigned in the event that a telephone interview would expedite consideration of the application.

Respectfully submitted,

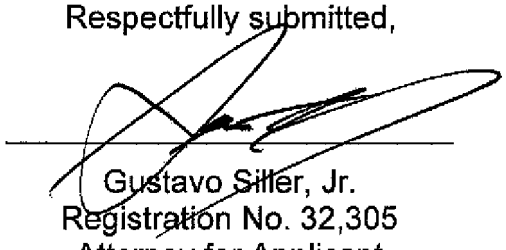

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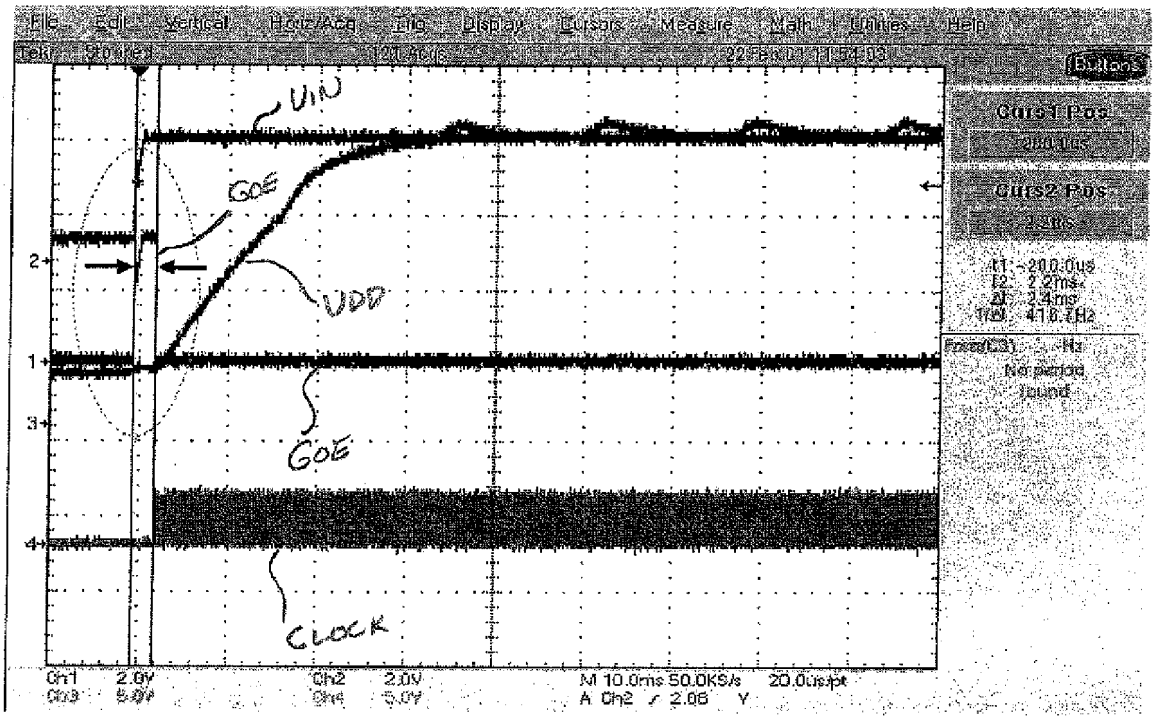
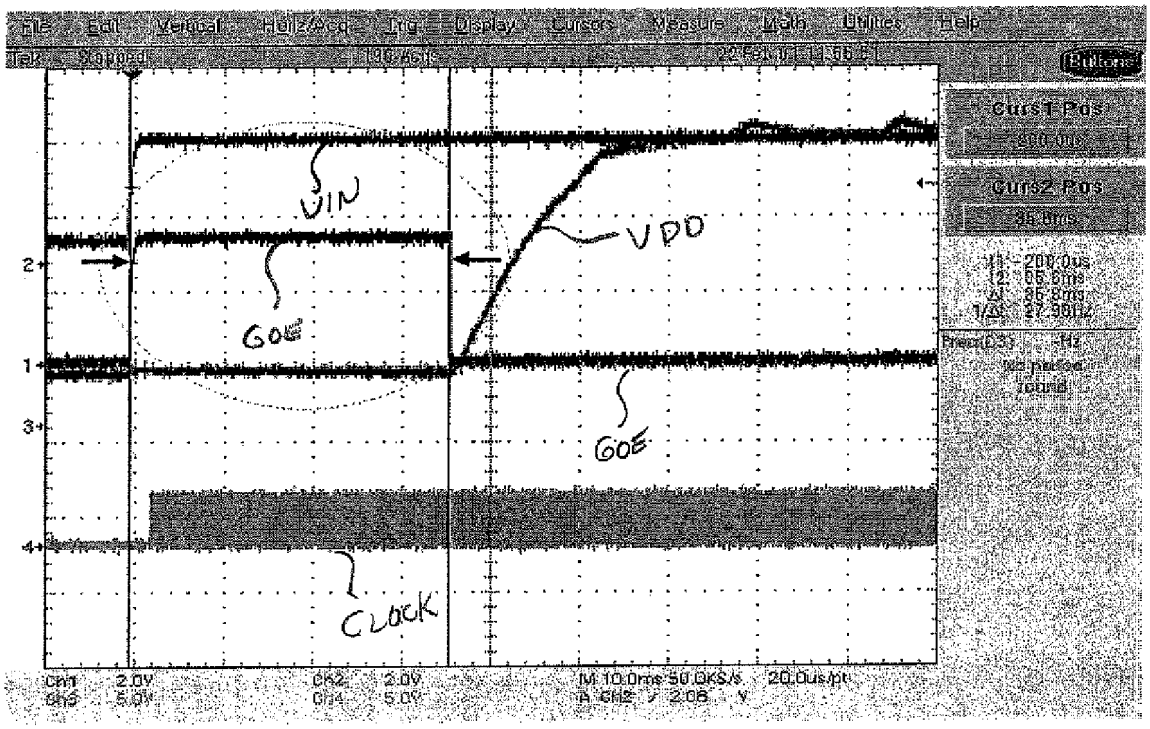
FIG. 5

Related Art



ADDING REFERENCES: VIN, GOE, VDD, and CLOCK

FIG. 8



ADDING REFERENCES: VIN, GOE, VDD, GOE, CLOCK